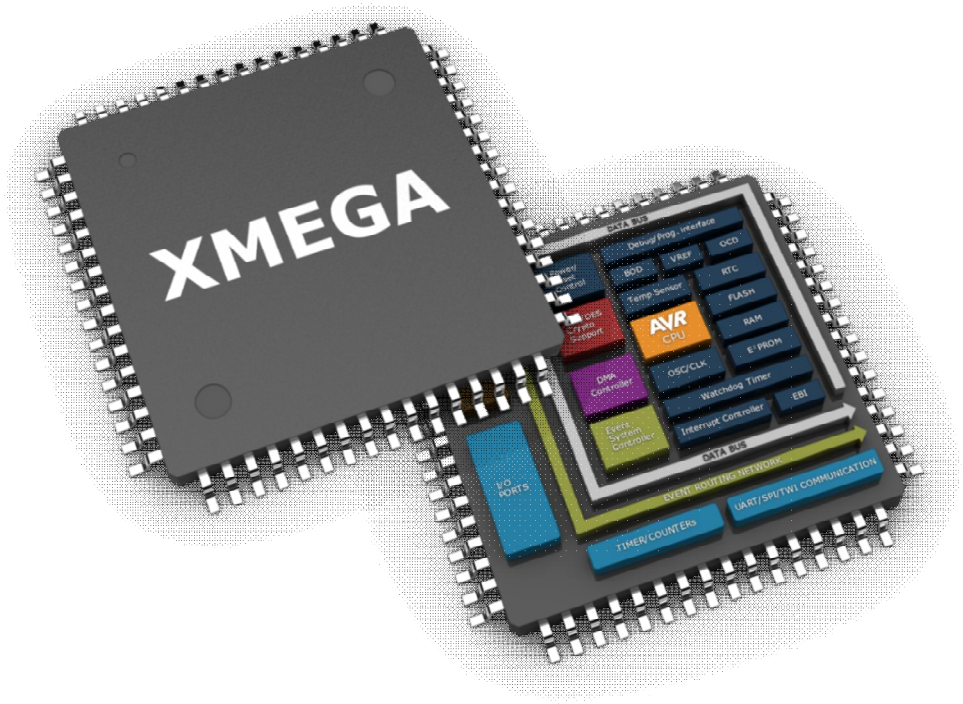


AVR® XMEGA™

Product Introduction

http://www.atmel.com

AVR Flash Microcontrollers

32-bit AVR UC3

The highest performance AVR in the world

8/16-bit AVR XMEGA

Peripheral Performance

8-bit megaAVR

The world's most successful MCU family

8-bit tinyAVR

Small packages, big performance

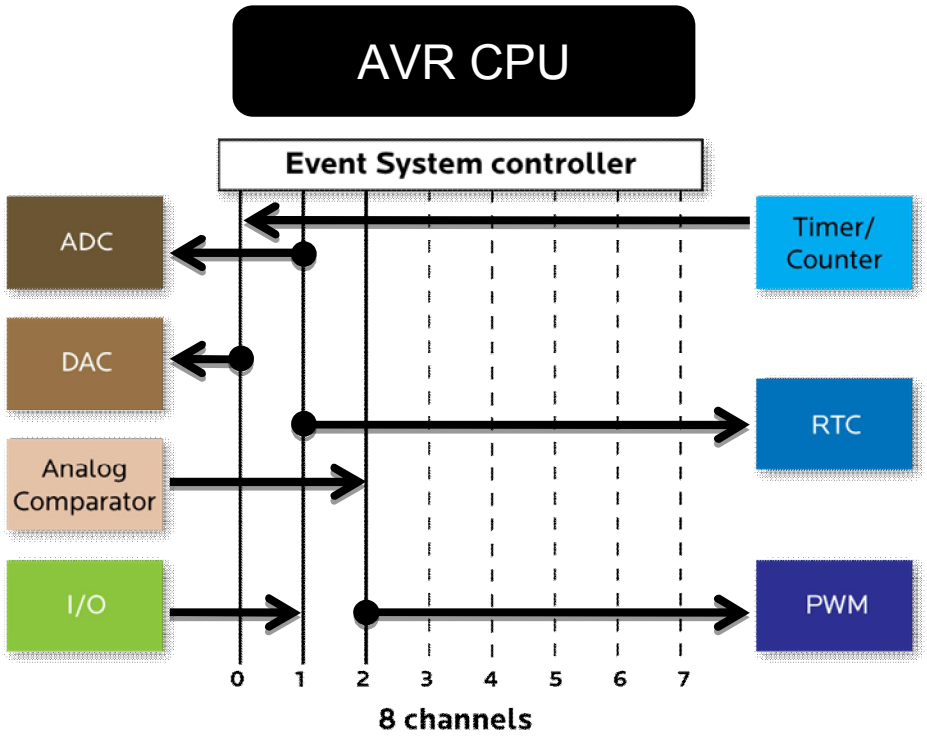
2nd generation picoPower

- **Industry leading in low power applications**

- **True 1.6V operation**
  - **Flash, Analog, EEPROM, Oscillators down**
  - **Enable 1.8V +/-10% power supply**
- **Lowest power 32 kHz Crystal Oscillator**
  - **550nA RTC**
- **Low leakage Process Technology**
  - **100nA for all devices**
- **1 µA Watchdog and Brown-Out**

Event System

- **Inter-peripheral communication**
  - **CPU and DMA independent**
- **Latency free**
  - **Safe fault protection**
  - **100% predictable reaction time**
- **Reduces power consumption**
  - **Zero CPU cycles needed**
- **8 channels**
  - **8 simultaneous events**

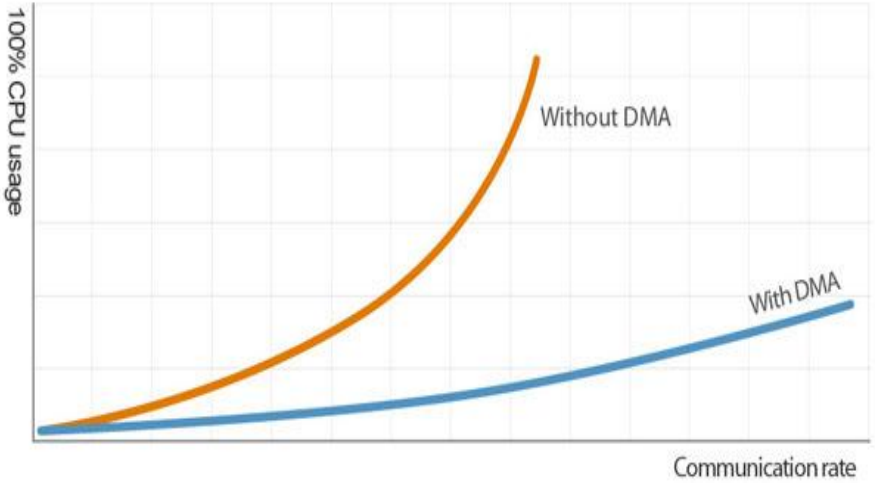


XMEGA DMA Controller

- **Allows high-speed data transfer**
  - **Works betweeen all combinations of peripherals and data memory**
  - **4 independent DMA channels**

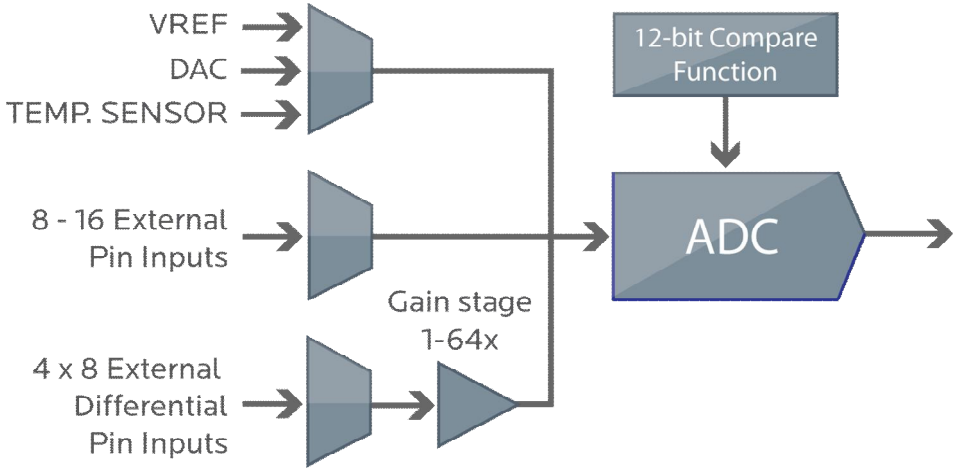
- **Remove high-speed bottlenecks**
- **Offload CPU for all data transfer**

CPU Load, UART or SPI Communication		
Data rate	With DMA	No DMA
250 kbps	0 %	8 %
500 kbps	0 %	16 %
1 Mbps	1 %	30 %
2 Mbps	1 %	57 %
4 Mbps	2 %	98 %



Leading Analog Integration

- **Up to 2 MSPS 12-bit ADC**
  - **Built in gain stage**
- **Up to 1 MSPS 12-bit DAC**
  - **Removes external DAC and filters**



- **Up to 4 Analog Comparators with window mode**
- **> 4kV HBD ESD**
  - **Reduced need for external protection**
- **±1% Internal Oscillators**
  - **Communication can run from internal RC**

Crypto Performance

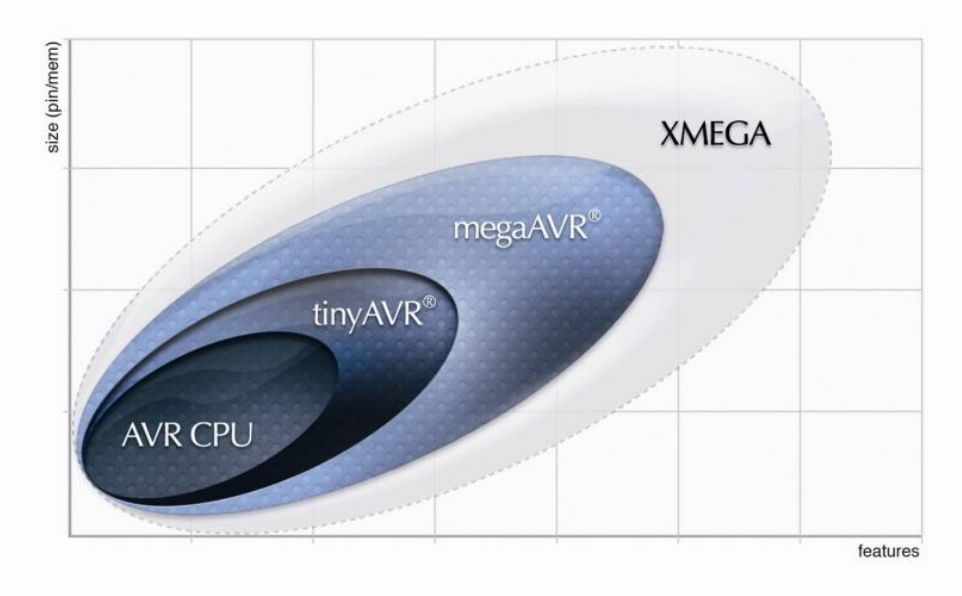
- **AES an DES crypto for high speed encrypted communication**
  - **Offload CPU and reduce power**

Max encrypted communication rate	UART	SPI	Vs. Software
128-bit AES	4 Mbps	3.2 Mbps	10x faster
Tripple-DES	3.2 Mbps	2.3 Mbps	100x faster

- **XMEGA with crypto is authorized for export to all countries**
  - **ECCN 5A002A.1**
- **XMEGA enables crypto communication for low power applications**

Compatibility and Migration

- **Same AVR CPU in tinyAVR, megaAVR and XMEGA**
  - **Reuse existing code**
  - **Reuse existing development tools**
- **AVR covers entire 8/16 bit market**
- **All XMEGA are code compatible**
  - **Develop with any XMEGA**
  - **Device selection at later stage**



XMEGA Device and Feature Overview

- **Wide device and integration selection over one compatible family**

AVR CPU @ 32 MHz	XMEGA A1	Up to 384 KBytes Flash	Up to 32 KBytes SRAM	Up to 4 KBytes EEPROM	8-channel Event Sys.	4-channel DMA Controller	8 USART 4 SPI 4 TWI	8x 16-bit T/C 24x PWM ch.	4x AC	2x 8-channel 2 MSPS 12-bit ADC	2x 2-channel 1 MSPS 12-bit DAC	AES, DES Crypto	EBI, Up to 16 Mbytes SRAM 128 Mbit SDRAM	100-lead TQFP 100-ball CBGA 100-ball VFBGA
Operating Voltage 1.6-3.6V	XMEGA A3	Up to 256 KBytes Flash	Up to 16 KBytes SRAM	Up to 4 KBytes EEPROM	8-channel Event Sys.	4-channel DMA Controller	7 USART 3 SPI 2 TWI	7x 16-bit T/C 22x PWM ch.	4x AC	2x 8-channel 2 MSPS 12-bit ADC	1x 2-channel 1 MSPS 12-bit DAC	AES, DES Crypto		64-lead TQFP 64-pad QFN
Memory Flash, SRAM, EEPROM Bootloader section	XMEGA A4	Up to 128 KBytes Flash	Up to 8 KBytes SRAM	Up to 2 KBytes EEPROM	8-channel Event Sys.	4-channel DMA Controller	5 USART 5 SPI 2 TWI	5x 16-bit T/C 24x PWM ch.	2x AC	1x 12-channel 2 MSPS 12-bit ADC	1x 2-channel 1 MSPS 12-bit DAC	AES, DES Crypto		44-lead TQFP 44-pad VQFN 49-ball VFBGA
Comm Intrefaces USART, SPI, TWI, IrDA	XMEGA D3	Up to 256 KBytes Flash	Up to 16 KBytes SRAM	Up to 4 KBytes EEPROM	4-channel Event Sys.		3 USART 2 SPI 2 TWI	5x 16-bit T/C 18x PWM ch.	2x AC	1x 16-channel 200 KSPS 16-bit ADC				64-lead TQFP 64-pad QFN
Event System	XMEGA D4	Up to 128 KBytes Flash	Up to 8 KBytes SRAM	Up to 2 KBytes EEPROM	4-channel Event Sys.		2 USART 2 SPI 2 TWI	4x 16-bit T/C 14x PWM ch.	2x AC	1x 12-channel 200 KSPS 12-bit ADC				44-lead TQFP 44-pad VQFN 49-ball VFBGA
16-bit T/C														
16-bit RTC														
12-bit ADC														
Analog Comparator														
Highly Configurable I/O														
+/-1% Accuarate Int. RC Osc.														
Power-on Reset Programmable BOD Programmable WDT														

Abbreviations:

T/C	Timer/Counter
RTC	Real Time Counter
ADC	Analog to Digital Converter
AC	Analog Comparator
DAC	Digital to Aanalog Controller
BOD	Brown-out Detection
WDT	Watch-Dog Timer
DMA	Direct Memory Access
EBI	External Bus Interface

- Included in all XMEGA devices
- Memory
- High performance
- Communication Interfaces
- Analog
- Crypto Engine
- EBI
- Package options

AVR XMEGA Roadmap

XMEGA A
DMA, Event System, Crypto
2 Msps ADC, 1 Msps DAC, AC
USART, TWI, SPI, 16-bit T/C,

XMEGA D
Event System
200 ksps ADC, AC
USART, TWI, SPI, 16-bit T/C

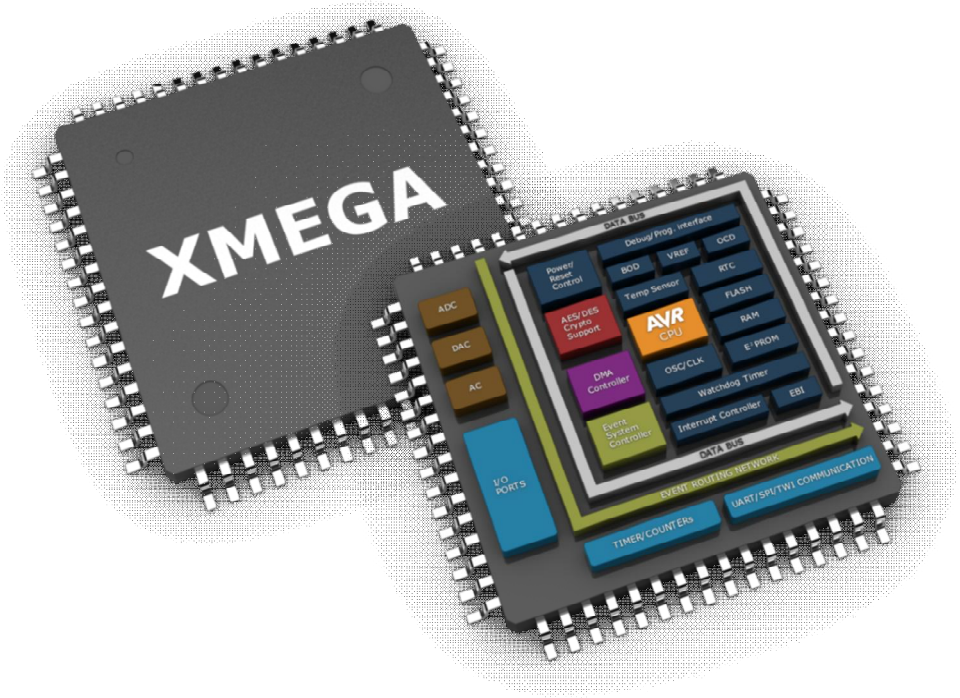
Flash	44	64	100	44	64	100
384 kB			384A1 Q4/11			
256 kB		256A3, 256A3B	256A1 Q4/11		256D3	
192 kB		192A3	192A1 Q4/11		192D3	
128 kB	128A4 Q2/11	128A3	128A1	128D4 Q2/11	128D3	
64 kB	64A4 Q2/11	64A3	64A1	64D4 Q2/11	64D3	
32 kB	32A4			32D4		
16 kB	16A4			16D4		

Pins

In Production

In Development
Sampling Date

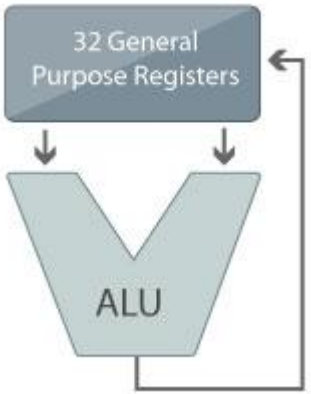
http://www.atmel.com



AVR XMEGA Technical Walk-Through

XMEGA AVR CPU

- **AVR CPU**
  - **Harvard architecture**
  - **True single cycle execution**
  - **32 MIPS at 32 MHz**
    - **32 MHz 2.7V – 3.6V**
    - **12 MHz 1.6V – 3.6V**
  - **32 General Purpose registers**

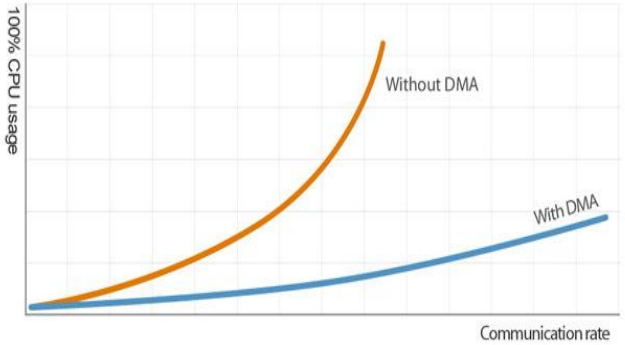


- **Adds DMA Controller**
- **Adds flexible Event System**
- **Adds Programmable Multi level Interrupt Controller**

XMEGA DMA Controller

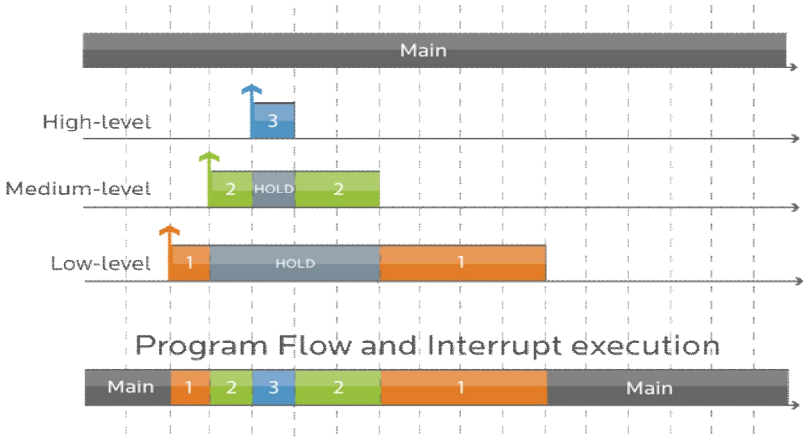
- **Allows high-speed data transfer**
  - From memory to peripheral
  - From memory to memory
  - From peripheral to memory
  - From peripheral to peripheral
- **Main features**
  - 4 channels
  - From 1 byte to 16 Mbyte transfers
  - Optional interrupt at end of transaction
  - Multiple addressing modes
    - Static, Increment, Decrement
  - 1, 2, 4 or 8 byte bursts
  - Programmable priority between channels

CPU Load, SPI Communication		
Data rate	With DMA	No DMA
250 kbps	0 %	8 %
500 kbps	0 %	16 %
1 Mbps	1 %	30 %
2 Mbps	1 %	57 %
4 Mbps	2 %	98 %



XMEGA Interrupt Controller

- 4 interrupt levels
  - NMI - Non Maskable Interrupts
  - High, Medium and Low level
  - Higher level will interrupt lower level interrupt service routines



- User selectable interrupt level for each interrupts source
- Round robin priority possible for low level interrupts
  - Ensures all interrupts are serviced
- All peripherals can also be controlled by polling

XMEGA Memories

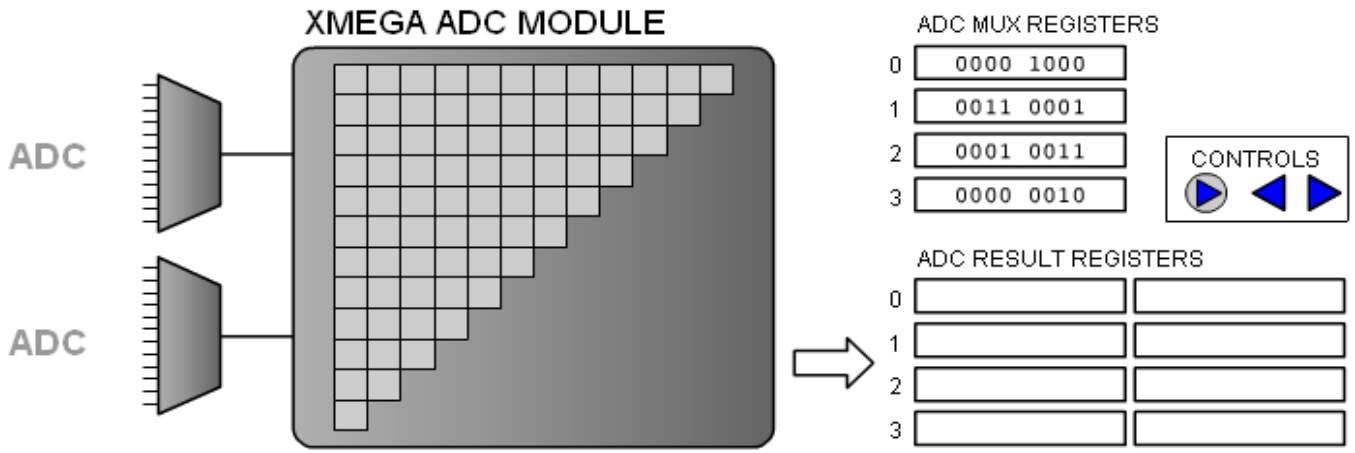
- **Flash**
  - Application area for main program
  - Boot area for bootloader
  - Application Table area for fail safe EEPROM emulation
- **EEPROM**
  - EEPROM on all devices
  - Byte and page accessible
  - Optional memory mapped
- **SRAM**
  - Internal on all devices
  - Optional external on some devices
    - Up to 16 MB directly addressable
    - Optional multiplexed address and data
- **Memory setup**

Flash	SRAM	EEPROM
16K + 4K	2K	1K
32K + 4K	4K	1K
64K + 4K	4K	1K
128K + 8K	8K	2K
256K + 8K	16K	4K

- **SDRAM**
  - Optional external on some devices
    - Up to 128 Mbit directly addressable
    - 4-bit and 8-bit supported

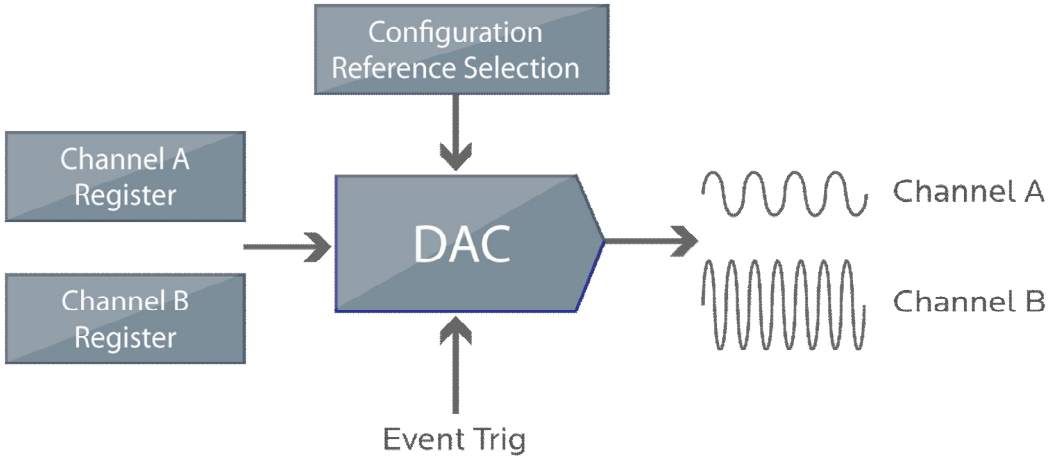
XMEGA ADC – Pipelining 4 Channels

- 4 ADC channels
- 8 – 12 external single-ended inputs per ADC
- 8 x 4 external differential inputs per ADC
- 4 internal inputs
  - VCC, Bandgap, Temperature, DAC output
- 1x, 2x, 4x, 8x, 16x, 32x or 64x gain
- Synchronous sampling in dual ADC devices



XMEGA Digital to Analog Converter

- **Features:**
  - **12 bit resolution**
  - **Up to 1 MSPS conversion rate, 1 µs settling time**
  - **Connected to Event System**
  - **Connected to DMA Controller**
  - **Two independent output channels per DAC**



XMEGA Analog Comparators

- **Selectable hysteresis**
  - **0, 20mV, 50mV selectable**
- **Flexible input selections**
  - **Any analog input pin**
  - **Output from DAC**
  - **Bandgap voltage reference**
  - **64-level VCC scaler**
- **Flexible interrupts and events generation**
- **Window compare function by combining 2 comparators**
  - **Detect level inside or outside window**
- **Possible to have comparator output on a pin**

XMEGA Timer/Counter

- **Multiple 16-bit Timer/Counters in each device**
  - Counts chip clock (Timer) or events (Counter)
  - 4 or 2Output Compare on each Timer/Counter
  - 4 or 2 Input Capture on each Timer/Counter
  - Programmable Top Value
  - Direction control
  - Flexible interrupts and events generation

- **High-Resolution Extension**
  - 4x of chip clock = up to 128 MHz operation
- **Advanced Waveform Extension**
  - Inverted and Non-inverted PWM Outputs
  - Dead Time Insertion
  - Fault protection mechanism
  - Available in all devices, but on 1-2 timer/counters only

XMEGA Serial Communication Modules

- **USART**
  - Full duplex asynchronous or synchronous operation
  - Can also be SPI master
  - Baud Rate Generator with fractional divider
    - UART frequency crystals not needed
- **SPI – Serial Peripheral Interface**
  - Full duplex, three-wire synchronous data transfer
- **TWI – Two Wire Interface**
  - I2C compatible
  - SMbus compatible
  - Fast data rate on slow chip clock
    - Clock / 10 for master operation
    - Asynchronous slave operation

XMEGA Crypto engine

- **AES**
  - **128-bit key length**
  - **Encryption of 16 bytes in 375 clock cycles**
  - **Decryption of 16 bytes in 375 clock cycles**

- **DES**
  - **56-bit key length**
  - **Encryption of 8 bytes in 16 clock cycles**
  - **Decryption of 8 bytes in 16 clock cycles**

- **Supports up to 4 Mbps AES encrypted communication**
- **Supports up to 3.2 Mbps Tripple-DES encrypted communication**

XMEGA Real Time Counter

- **Separate Timer for Asynchronous Clock**
  - **Independent of other Timer/Counters**
  - **Works in Power Save, Idle and Active mode**
- **16-bit timer with Programmable Prescaler**
  - **Prescaler provides 1 Hz – 32 kHz input**
  - **Programmable top value**
  - **Compare register**
  - **Max timeout 65 536 seconds (= more than 18 hours)**
- **Can generate Events and Interrupts**
  - **Both overflow and compare match**

XMEGA Clock Options

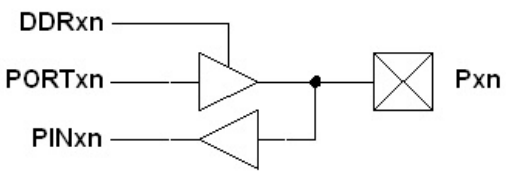
- 32- and 2 MHz internal RC osc.
  - +/- 1% accuracy over temp and voltage with automatic run-time calibration
- 32.768 kHz internal RC osc.
  - +/- 2% accuracy over temp and voltage
- 400 kHz – 16 MHz Crystal osc.
  - For accurate timing in application
- 32.768 kHz Crystal oscillator
  - for 32 kHz watch crystal
  - 500 nA current consumption
- 32 kHz ULP RC oscillator
  - For WDT and BOD
  - 1μA power consumption
- Internal PLL for high-freq clock generation
  - 400 kHz – 32 MHz input
  - 8 – 128 MHz output
  - Max 32 MHz output to main system clock

XMEGA I/O Pins

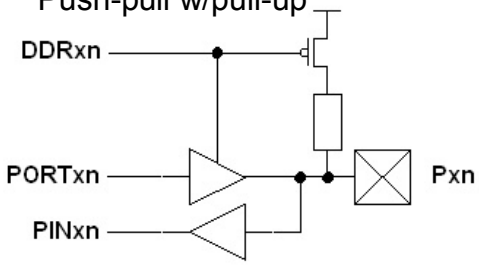
- **IN, OUT and DIR registers for safe read modify write operations**
- **Virtual registers for easy pin manipulation**
  - **Move IN, OUT and DIR control to bit addressable memory area**
  - **Port Toggle, Clear and Set registers for easy and glitch free pin manip**

- **Advanced pin configurations**

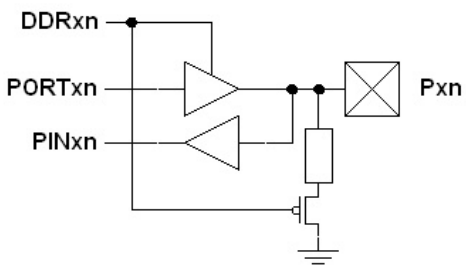
Push-pull



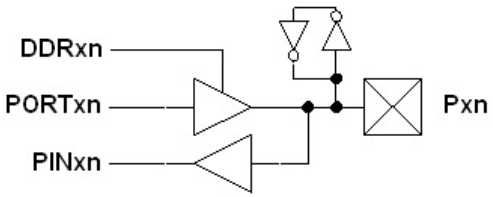
Push-pull w/pull-up



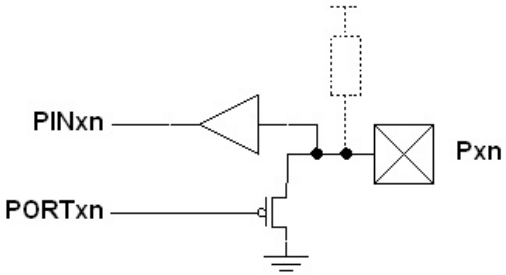
Push-pull w/pull-down



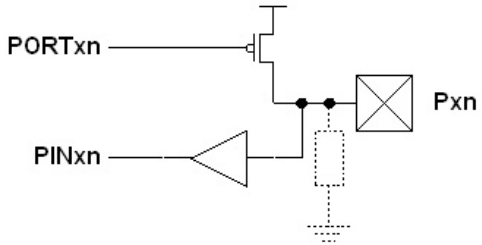
Push-pull w/ buskeeper



Wired AND w/ optional pull-up



Wired OR w/ optional pull-down



2nd generation picoPower

- All picoPower features included
- New sampled BOD
- New low power Watchdog Timer
- New Event system controls peripherals in Idle mode
- New DMA moves data in Idle mode

- Lowest power consumption
  - 100 nA Power Down (RAM retention)
  - 550 nA Power Save (Real Time Counter)
  - 5 µs wake-up from sleep

5 Sleep Modes

- **Idle**
  - All peripherals run as normal. No code can run
  - Any peripheral can wake device
  - DMA Controller and Event system still working
- **Power save**
  - Asynchronous clock operating. Only RTC can run
  - Real Time Clock, External Interrupts, TWI Address Match and Watchdog Timer can wake the device
- **Power down**
  - No clocks running. No operation
  - External Interrupts, TWI Address Match and Watchdog Timer can wake the device
- **Standby**
  - Power down, but oscillator is running for fast wake-up
- **Extended standby**
  - Power save, but oscillator is running for fast wake-up

XMEGA Special Features

- Calibration memory
  - Readable from application
  - Factory calibration
  - User calibration
    - Can be modified by customer
  - Not affected by Chip Erase or SPM
- Serial numbers
  - Unique identifier
  - Random number seed
- Dynamic Clock Switching
- Oscillator failure detection
- Memory lock bits
- Brown-Out Detector
  - Very fast
  - Low power
  - Off, 1 kHz sampled or On
- Watchdog Timer
  - Separate oscillator
- Clock generation
  - Clock output
- CRC checksums
  - Available on locked devices